



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/915,311 | 07/27/2001 | Masahiro Kiyoi | NIT-285 | 5904 |

24956 7590 04/11/2005

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

| |
|----------|
| EXAMINER |
|----------|

MASKULINSKI, MICHAEL C

| | |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2113

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/915,311

Applicant(s)

KIYOI ET AL.

Examiner

Michael C Maskulinski

Art Unit

2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-11 is/are allowed.
- 6) ☒ Claim(s) 1,2 and 4 is/are rejected.
- 7) ☒ Claim(s) 3 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Final Office Action

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagasuka et al., U.S. Patent 6,615,364 B1.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Referring to claim 1:

a. In column 3, lines 20-25, Nagasuka et al. disclose that the external storage unit is used as a paging device unit. The paging device includes a primary paging device unit used as a paging device unit during a normal operation and a secondary paging device unit used as a substitution (providing said auxiliary storage with first auxiliary storage and second auxiliary storage and operating the computer system using either of the first auxiliary storage or the second auxiliary storage)

b. In column 3, lines 48-52, Nagasuka et al. disclose that the paging process is a process of outputting data in the main memory in an area having a small

access frequency to the paging device unit when a use factor of the main memory becomes high and an empty area becomes small (transferring content of the virtual-storage area on the main storage from the main storage to the auxiliary storage when a utilization ratio of the main storage becomes high).

c. In column 3, lines 4-10, Nagasuka et al. disclose that the control register holds various control information such as a start real address of an address translation table to be used for accessing the virtual memory (determining a location to which the address translation table is allocated when occurrence of a failure in the computer system is detected).

d. In column 4, lines 9-16, Nagasuka et al. disclose that areas of the virtual memory are allocated in the page unit to the main memory or primary paging device unit (determining a location in the main storage, or in the auxiliary storage, where information in the virtual-storage area is stored, which is described in the address translation table).

e. In column 3, lines 52-55, Nagasuka et al. disclose a process of inputting data in a virtual memory area in the main memory if the data in the virtual memory to be accessed by CPU was output to the paging device unit. Because Nagasuka et al. disclose a process of retrieving data from the paging device unit that was in virtual memory, then the process of transferring the content of the virtual-storage area from the main storage to the auxiliary storage to which the content of the virtual-storage area is allocated when the utilization ratio of the

Art Unit: 2113

main storage becomes high, if the content of the virtual-storage area is allocated to the main storage had to inherently occur.

f. In column 3, lines 56-65 continued in column 4, lines 1-5, Nagasuka et al. disclose that the switching process is called and executed when the main memory information acquiring process is completed. The switching process acquires the identifier of the external storage unit currently used as the paging device unit from the configuration information and changes the setting of the identifier of an external storage unit so that the secondary paging device is used as the primary paging device unit when the computer system restarts (switching the first auxiliary storage to the second auxiliary storage for use if the first auxiliary storage is used for operation, or switching the second auxiliary storage to the first auxiliary storage for use if the second auxiliary storage is used for operation).

Referring to claim 2, in column 4, lines 40-47, Nagasuka et al. disclose that the invalid bit indicates whether the real address is invalid or not. If the invalid bit is set to "1", it means that the real address is invalid. More specifically, the page of the virtual memory corresponding to this entry is not used or data in this page was paged out into the primary paging device unit at the page-out destination address (from among the virtual-storage pages that have been allocated to the main storage, only areas, which have been updated since the areas were allocated to the main storage, are extracted, and are then transferred from the main storage to the auxiliary storage).

Referring to claim 4:

- a. In column 3, lines 20-25, Nagasuka et al. disclose that the external storage unit is used as a paging device unit. The paging device includes a primary paging device unit used as a paging device unit during a normal operation and a secondary paging device unit used as a substitution (providing said auxiliary storage with first auxiliary storage and second auxiliary storage and operating the computer system using either of the first auxiliary storage or the second auxiliary storage).
- b. In column 3, lines 48-52, Nagasuka et al. disclose that the paging process is a process of outputting data in the main memory in an area having a small access frequency to the paging device unit when a use factor of the main memory becomes high and an empty area becomes small (transferring content of the virtual-storage area on the main storage from the main storage to the auxiliary storage when a utilization ratio of the main storage becomes high).
- c. In column 3, lines 4-10, Nagasuka et al. disclose that the control register holds various control information such as a start real address of an address translation table to be used for accessing the virtual memory (determining a location to which the address translation table is allocated when occurrence of a failure in the computer system is detected).
- d. In column 4, lines 9-16, Nagasuka et al. disclose that areas of the virtual memory are allocated in the page unit to the main memory or primary paging device unit (determining a location in the main storage, or in the auxiliary storage,

where information in the virtual-storage area is stored, which is described in the address translation table).

e. In column 3, lines 52-55, Nagasuka et al. disclose a process of inputting data in a virtual memory area in the main memory if the data in the virtual memory to be accessed by CPU was output to the paging device unit. Because Nagasuka et al. disclose a process of retrieving data from the paging device unit that was in virtual memory, then the process of transferring the content of the virtual-storage area from the main storage to the auxiliary storage to which the content of the virtual-storage area is allocated when the utilization ratio of the main storage becomes high, if the content of the virtual-storage area is allocated to the main storage had to inherently occur. Further, in column 4, lines 40-47, Nagasuka et al. disclose that the invalid bit indicates whether the real address is invalid or not. If the invalid bit is set to "1", it means that the real address is invalid. More specifically, the page of the virtual memory corresponding to this entry is not used or data in this page was paged out into the primary paging device unit at the page-out destination address (if the content of the virtual-storage area has been updated since the virtual-storage area was allocated to the main storage).

f. In column 3, lines 56-65 continued in column 4, lines 1-5, Nagasuka et al. disclose that the switching process is called and executed when the main memory information acquiring process is completed. The switching process acquires the identifier of the external storage unit currently used as the paging

device unit from the configuration information and changes the setting of the identifier of an external storage unit so that the secondary paging device is used as the primary paging device unit when the computer system restarts (switching the first auxiliary storage to the second auxiliary storage for use if the first auxiliary storage is used for operation, or switching the second auxiliary storage to the first auxiliary storage for use if the second auxiliary storage is used for operation).

Allowable Subject Matter

3. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 5-11 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

Referring to claim 5, the prior art does not teach or reasonably suggest a means for transferring content of the virtual-storage area from the main storage to the auxiliary storage according to the address translation table when occurrence of a failure in the computer system is detected in combination with the other limitations of the claim.

Referring to claim 6, the prior art does not teach or reasonably suggest storing the content of the virtual-storage area, which has been updated since the virtual-storage area was allocated to the main storage, in the first auxiliary storage according to the

Art Unit: 2113

address translation table when occurrence of a failure in the computer system is detected in combination with the other limitations of the claim.

Referring to claim 7, the prior art does not teach or reasonably suggest storing content in each area of the plurality of pieces of virtual storage, which has been updated since the area of the virtual storage was allocated to the main storage, in the first auxiliary storage according to the address translation table when occurrence of a failure in the computer system is detected in combination with the other limitations of the claim.

Referring to claims 8 and 9, the prior art does not teach or reasonably suggest restoring the address translation table, which has been saved in the first auxiliary storage, in the main storage before switching the first auxiliary storage, which is working, to second auxiliary storage.

Referring to claims 10 and 11, the prior art does not teach or reasonably suggest a processing part to output, when a failure occurs, the information in said main storage among the information in said virtual-storage area to said auxiliary storage to which said information in said main storage is output when the utilization ratio of said main storage becomes high.

Response to Arguments

6. Applicant's arguments filed January 19, 2005 have been fully considered but they are not persuasive.

7. On pages 16-17, under the section Comparison Between the Present Invention and Cited Reference, the Applicant argues, "Nagasuka et al. do not disclose that when occurrence of a failure in the computer system is detected, if the content of the virtual-

Art Unit: 2113

storage area is allocated to the main storage, the content of the virtual-storage area is output from the main storage to the auxiliary storage to which the content of said virtual-storage area is allocated when the utilization ratio of the main storage becomes high, as set forth in claims 1, and 4-7 of the present application.” The Examiner respectfully disagrees. The Examiner would like to note that the he understands the arguments and differences shown by the Applicant, however, the claim language of claims 1 and 4, states that when there is an occurrence of a failure the only action performed is determining a location to which the address translation table is allocated. For this reason, the Examiner has made the above rejection. The Examiner suggests either canceling these claims or amending them to include the claim language of claims 5-11.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Art Unit: 2113

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM


ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100